WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit including an interface circuit which receives a relatively high first voltage and a relatively low second voltage as power supply voltages, and suspends operation of the interface circuit in a non-access mode so that an external access is not executed by shutting off supply of the first voltage to be applied to the interface circuit that receives an externally supplied signal, the interface circuit comprising:

an input buffer that operates by applying at least the first voltage as the power supply voltage;

a transfer gate that is coupled to and between an external input terminal and an input end of the input buffer, and that transmits an external signal input from the external input terminal to the input end of the input buffer; and

a gate voltage control circuit that outputs a gate voltage to be applied to a gate electrode of the transfer gate, the gate voltage control circuit outputting a voltage produced based on the first voltage as the gate voltage in an access mode so that an external access is executed while outputting a voltage produced based on the second voltage as the gate voltage in the non-access mode.

2. The semiconductor integrated circuit according to Claim 1, the gate voltage control circuit comprising four (4) p-type MOS transistors formed in a same n-type substrate region,

a first p-type MOS transistor comprising a source electrode, to which the first voltage is applied, and a drain electrode, to which the gate electrode of the transfer gate is coupled, and turns on in the access mode so as to output a voltage almost equal to the first voltage to the gate electrode of the transfer gate;

a second p-type MOS transistor comprising a source electrode, to which the second voltage is applied, and a drain electrode, to which the gate electrode of the transfer gate is coupled, and turns on in the non-access mode so as to output a voltage almost equal to the second voltage to the gate electrode of the transfer gate;

a third p-type MOS transistor comprising a source electrode, to which the first voltage is applied, and a drain electrode, to which a first electrode in the n-type substrate region is coupled, and turns on in the access mode, thereby performing charging such that a potential of the n-type substrate region becomes almost equal to the first voltage; and

a fourth p-type MOS transistor comprising a source electrode, to which the second voltage is applied, and a drain electrode, to which a second electrode in the n-type substrate region is coupled, and turns on in the non-access mode, thereby performing charging

such that the potential of the n-type substrate region becomes almost equal to the second voltage.

3. The semiconductor integrated circuit according to Claim 1,

each MOS transistor forming the interface circuit being an MOS transistor in which a maximum rated voltage at a gate electrode is greater than the first voltage and lower than a third voltage corresponding to a high level voltage of the external signal, and

the second voltage being set such that a voltage difference between the third voltage and the second voltage is lower than the maximum rated voltage.

4. The semiconductor integrated circuit according to Claim 1, the first voltage being in the range from 3V to 3.6V, the second voltage being in the range from 1.65V to 1.95V, and the third voltage being in the range a voltage from 4.5V to 5.5V.

5. The semiconductor integrated circuit according to Claim 2,

each MOS transistor forming the interface circuit being an MOS transistor in which a maximum rated voltage at a gate electrode is greater than the first voltage and lower than a third voltage corresponding to a high level voltage of the external signal, and

the second voltage being set such that a voltage difference between the third voltage and the second voltage is lower than the maximum rated voltage.

6. The semiconductor integrated circuit according to Claim 2, the first voltage being in the range from 3V to 3.6V, the second voltage being in the range from 1.65V to 1.95V, and the third voltage being in the range a voltage from 4.5V to 5.5V.